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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,477	09/23/2003	Kenneth Graham Paterson	B-3719DIVofPCT 621147-1	4835

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EXAMINER	
CHUNG, DANIEL J	
ART UNIT	**PAPER NUMBER**
2677	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,477	PATERSON, KENNETH GRAHAM	
	Examiner	Art Unit	
	Daniel J. Chung	2677	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 26-32 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 26-32 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

The drawings are approved by the Examiner.

Specification

Please review the application and correct all informalities.

Claim Objections

Claim 31 is objected to because of the following informalities: claim 31 is duplicated claim of claim 30. Applicant is respectfully requested to cancel claim 31. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 26-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (5,721,709)

Regarding claim 26, Nakamura discloses that the claimed feature of a decoder system, comprising: an address input [input buffer circuit; "IB"] for receiving an address signal representing any of a plurality of address values (d) [A0-A4]; a plurality of intermediate nodes [i.e. nodes between "PD" and "DEC" or nodes between "DEC" and "WD" in Fig 1]; a decoder responsive to the address signal and arranged to stimulate, for each address value [A0-A4], a respective combination of the intermediate nodes; and a plurality of outputs [WL0-WL31], each responsive to a respective group of the intermediate nodes such that the stimulation applied to that output is dependent upon the stimulation applied by the decoder to each of the intermediate nodes in the respective group; wherein the decoder is arranged to perform a plural-stage process ["plural-stage"; i.e. first stage thru fourth stage] in determining which of the intermediate nodes to stimulate in response to each address value [A0-A4], plural-stage process comprising at least a first stage [i.e. "PD" thru "DEC"] in which results are determined and a second stage [i.e. "DEC" thru "WD"] for which the results of the first stage are provided as inputs. (See Abstract, Fig 1, col 2 line 32-col 3 line 4, col 3 line 41-61, col 12 line 55-col 13 line 41)

Nakamura does not explicitly disclose that determining of a word of a predetermined constant weight code. However, this would have obvious to one having

ordinary skilled in the art at the time of Applicant's invention, in order to provide the process of decoding with detecting all single/multiple bit errors effectively, as such improvement is also advantageously desirable in the teaching of Nakamura for performing the decoder circuit at high speed with less errors being made.

Regarding claim 27, Nakamura does not explicitly teach that the decoder comprises a microprocessor which is programmed to perform the plural-stage process. However, it is inherent that some type of processor [i.e. microprocessor] is necessarily required for executing the decoder circuitry of Nakamura, which performs a multi-stage process. (See Fig 1, Abstract line 3-6, col 3 line 44-53)

Regarding claim 28, Nakamura discloses that hard-wired logic circuitry and/or arithmetic circuitry and/or look-up circuitry arranged to perform the plural-stage process. (See Fig 1, Abstract line 3-7, col 3 line 44-47)

Regarding claim 29, refer to the discussion for the claim 26 hereinabove, Nakamura does not explicitly disclose that determining of a word of a predetermined constant weight code. However, this would have obvious to one having ordinary skilled in the art at the time of Applicant's invention, in order to provide the process of decoding with detecting all single/multiple bit errors effectively, as such improvement is also

advantageously desirable in the teaching of Nakamura for performing the decoder circuit at high speed with less errors being made.

Regarding claim 30, Nakamura discloses that in response to each address value, a respective single one of the outputs [WL0-WL31] is stimulated, or stimulated beyond a predetermined threshold. (See Fig 1, col 13 line 20-23, col 14 line 10-14)

Regarding claim 32, Nakamura discloses that the claimed feature of a method of manufacturing a decoder system having the following elements: an address input [input buffer circuit; "IB"] for receiving an address signal representing any of a plurality of address values [A0-A4]; a plurality of intermediate nodes [nodes between "DEC" and "WD" in Fig 1]; a decoder responsive to the address signal and arranged to stimulate, for each address value, a respective combination of the intermediate nodes and a plurality of outputs [WL0-WL31], each responsive to a respective group of the intermediate nodes such that the stimulation applied to that output is dependent upon the stimulation applied by the decoder to each of the intermediate nodes in the respective group, wherein the decoder is arranged to perform a plural stage process ["plural-stage"; i.e. first stage thru fourth stage] in determining which of the intermediate nodes to stimulate in response to each address value, plural stage process comprising at least a first stage [i.e. "IB" thru "DEC"] in which results are determined and a second stage [i.e. "DEC" thru "WD"] for which the results of the first stage are provided as inputs; wherein the method of manufacturing comprises the steps of; providing such a

decoder which is; responsive to an address signal representing any of a plurality of address values and arranged to stimulate, for each address value, a respective combination of intermediate nodes; providing a plurality of output; determining, for each output, a respective group of the intermediate nodes to which that output is to be responsive and rendering each output responsive to the intermediate nodes in the respective determined group such that the stimulation applied to that output is dependent upon the stimulation applied by the decoder to each of the intermediate nodes in the respective group; characterized by the steps of; determining a plural stage process to be performed by a decoder, plural stage process comprising at least a first stage in which results are determined and a second stage for which the results of the first stage are provided as inputs; arranging the decoder to perform the determined plural stage process in determining which of the intermediate nodes to stimulate in response to each address value; and using the determined plural stage process in step of determining the group of the intermediate nodes to the outputs are to be responsive. (See Abstract, Fig 1, col 2 line 32-col 3 line 4, col 3 line 41-61, col 12 line 55-col 13 line 41)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Chung whose telephone number is (571) 272-7657. He can normally be reached Monday-Thursday and alternate Fridays from 7:30am- 5:00pm. If attempts to reach the examiner by

telephone are unsuccessful, the examiner's supervisor, Michael, Razavi, can be reached at (571) 272-7664.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

571-273-8300 (Central fax)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

djc
August 23, 2005

DENNIS-DOON CHOW
PRIMARY EXAMINER